

PE-xxxx  
Revision A

WS1050 MEMS CYCLING AND HOLD DOWN

TEST PROCEDURE

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# Purpose and Scope

## Purpose

This document defines the procedures and requirements for cycling and holding down stresses for MEMS capacitors.

## Scope

This procedure applies to the qualification and ongoing production monitoring of all WiSpry products.

# Responsibilities

The Product Engineering function is responsible for assuring compliance to the requirements of this document.

# REFERENCE DOCUMENTS

|  |  |
| --- | --- |
| Document No. | Document Name |
| PE-0002 | Equipment Calibration Procedure |

# FORMS

|  |  |
| --- | --- |
| Form No. | Form Name |
|  |  |

# DEFINITIONS (Not Applicable)

# EQUIPMENT AND MATERIALS

Equipment consists of:

|  |  |  |  |
| --- | --- | --- | --- |
| **Item** | **Model** | **Manufacturer** | **Comments** |
| Computer (equipment controller) | PC with Window XP, 7 | Any |  |
| Software (equipment controller) | LabView 2012 or Higher |  |  |
| GPIB-USB-HS | 778927-01 | National Instruments |  |
| Triple Output Power Supply | E3631A | Agilent/Keysight | w/ GBIP interface |
| Source Meter | 2400 | Keithley | w/ GBIP interface |
| DMM | 2000 | Keithley | w/GPIB interface |
| FPGA | PIX-7813R | National Instruments |  |
| PXI Card Chassis | PIX-1033 | National Instruments |  |
| DUT boards | Various**1** | --- | WiSpry Design |
| SHC68-68-RDIO Shielded Cable | 191667-01 | National Instruments | NI Cables |

Notes:

**1** WS1050 board is 36 positions (model WS-EVB-165)

# REQUIREMENTS AND PROCEDURES

## Basic Hardware, Software, and Environmental Requirements

* Cycling and hold down hardware (boards, cables, connectors, bench equipment) must be able to:
  + Meet the electrical conditions specified in sections 7.2 and 7.3.
  + Meet WiSpry calibration requirements specified in PE-0002.
  + Be sufficiently robust to ensure minimum leakage currents.
* Cycling and hold down software should:
  + Allow for insitu monitoring for stiction events.
  + Meet the electrical conditions specified in sections 7.2 and 7.3.
* Cycling and hold down environmental controls shall:
  + Provide control of temperature and humidity.
  + Meet calibration requirements defined in PE-0002.

## MEMS Cycling

The cycling conditions for product qualification and ongoing monitoring are:

|  |  |
| --- | --- |
| **Stress Condition** | **Requirement** |
| MEMS Operating Voltage (VOP) | 44 V |
| VDD | 3.7 V @ 12 KHz |
| Temperature | 65 oC |
| Frequency | 12 KHz |
| Duty Cycle | 25% |
| Dual Voltage Actuation (DVA) | OFF |
| Beam Actuation | All beams cycles simultaneously |

## MEMS Hold Down

The hold down conditions for product qualification and ongoing monitoring are:

|  |  |
| --- | --- |
| **Stress Condition** | **Requirement** |
| MEMS Operating Voltage (VOP) | 44 V |
| VDD | 3.3 V |
| Temperature | 65 oC |
| Frequency | ---- |
| Duty Cycle | 100% |
| Dual Voltage Actuation (DVA) | OFF |
| Beam Actuation | All beams cycles simultaneously and held for the stress duration |

## Reject Criteria

For both cycling and hold down, the following conditions define a reject reading:

COFF ±46 fF per bank

CON ±657 fF per bank

## General Set-up and Handling Guidelines

* Handling recommendations for ESD
* Stabilize oven temperature prior to loading parts, 15 minutes minimum
* Preconditioning of new stress boards (to remove excess moisture absorption), 24 hour bake at 85C
* Optimal method to load boards
* Special software instructions
* Best way to unload parts
* Socket inspection after each run and cleaning/repair as required
* Sample control and storage post stress

## Test Set-up Procedure

* Figure 1 shows the test set-up block diagram for WS1050 Reliability Test, Multi DUT.
* Using banana plug cables to connect all test equipments as in Figure 1.
* For power supply E3631A, use channel 1 for VDD, channel 2 for +3.3V.



**Figure 1 Test Set-up Block Diagram**

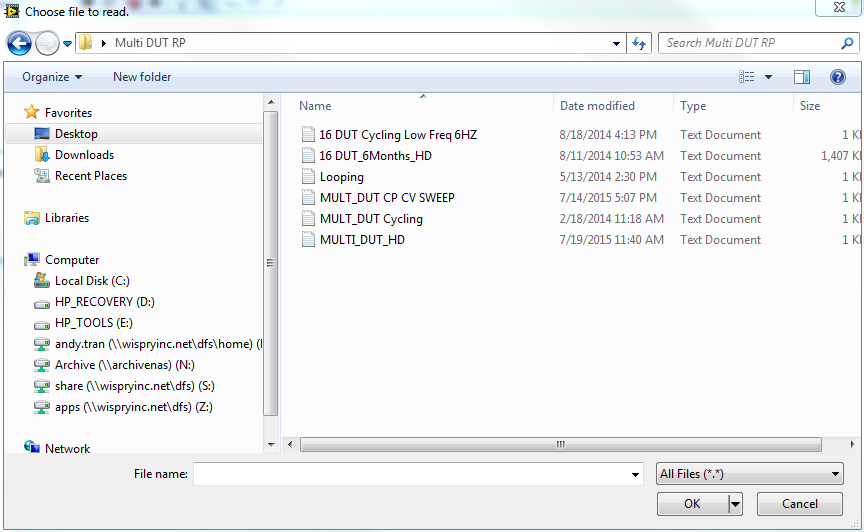
* Figure 2 shows the front panel of the test program (for the WS1050 version 1.4)
* Contact WiSpry Engineering for the latest version of the test program.
* Test programs are located in directory S:\Software\_Control\Released\36 DUT Board



**Figure 2**

## Test Operating Procedure

* Set temperature from oven/chamber
* Adjust temperatures from oven/chamber to meet the requirement (for example 25C, 45C, 65C)
* Set-up test program
* From labVIEW test program click  this button at the top left corner to run the test program, it will pop-up a dialog box (Figure 3) below to ask the look up table for read point

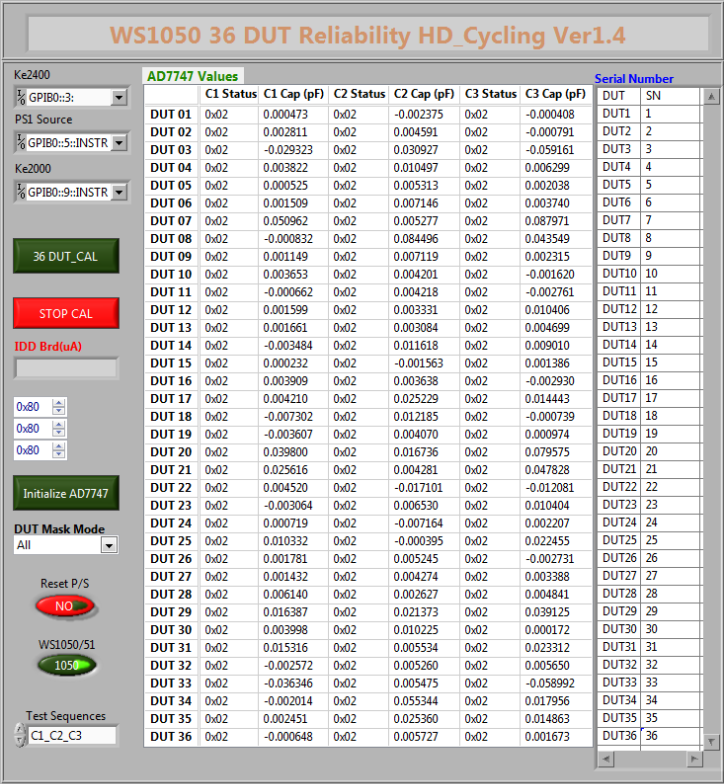


**Figure 3**

Note:

Selecting the correct file depends on the stress being run;

* + Select **MULT\_DUT Cycling** for cycling test
  + Select **MULT\_DUT HD** for hold down test
* For calibration (Figure 4): Make sure all sockets are empty and the capacitance values of 36 DUT are around zeros “~0”for all three banks. If not, click on 36 DUT\_CAL button  to zero out the sockets, then click STOP CAL button  to stop the calibration.



**Figure 4**

Note: If sockets are not zeros “~0”, click on initialize AD7747 button  to initialize the ADI chip, make sure the capacitance values will be less than 1pF (<1pF) for all three banks of 36 DUT, click on 36 DUT\_CAL button to zero out the sockets then click on STOP CAL button to stop the calibration.

* Set-up test condition (Fig. 5): The front panel below was set by default with cycling, DVA OFF, E-CAL OFF, VPI ON, VSA ON, HS (hand shake check) = ON, VDD = 3.7V, cycle speed = 12 KHz, CP stress = 40.25V, CP VPI = 35V.

# 

**Figure 5**

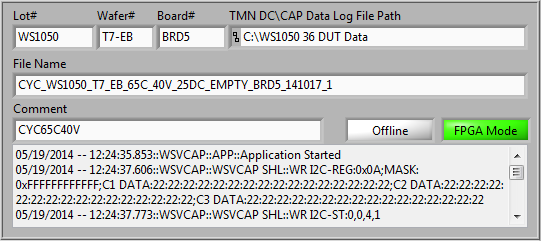
* Set-up with standard stress (cycle): All Drivers ON, All Drivers OFF, 25% Duty. Make sure the numbers will be set as same as the boxes are shown below**:**

# 

* Set-up with special stress (cycle): C1 ON, C2 OFF, C3 OFF; C1 OFF, C2 ON, C3 OFF; C1 OFF, C2 OFF, C3 ON, 33% Duty. Make sure all the numbers will be set as same as the boxes are shown below:

# 

* + Set-up for stress (Hold Down): All Drivers should be closed during hold down, 100% duty, this was set by default 
* Figure 6 shows the front panel is set-up to collect the test data.

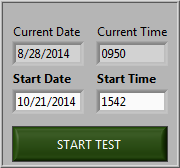


**Figure 6**

Note: The file name format will be…

**stress\_lot#\_wafer#\_design\_temperature\_CPV Stress\_duty\_brd#\_yymmdd\_run**

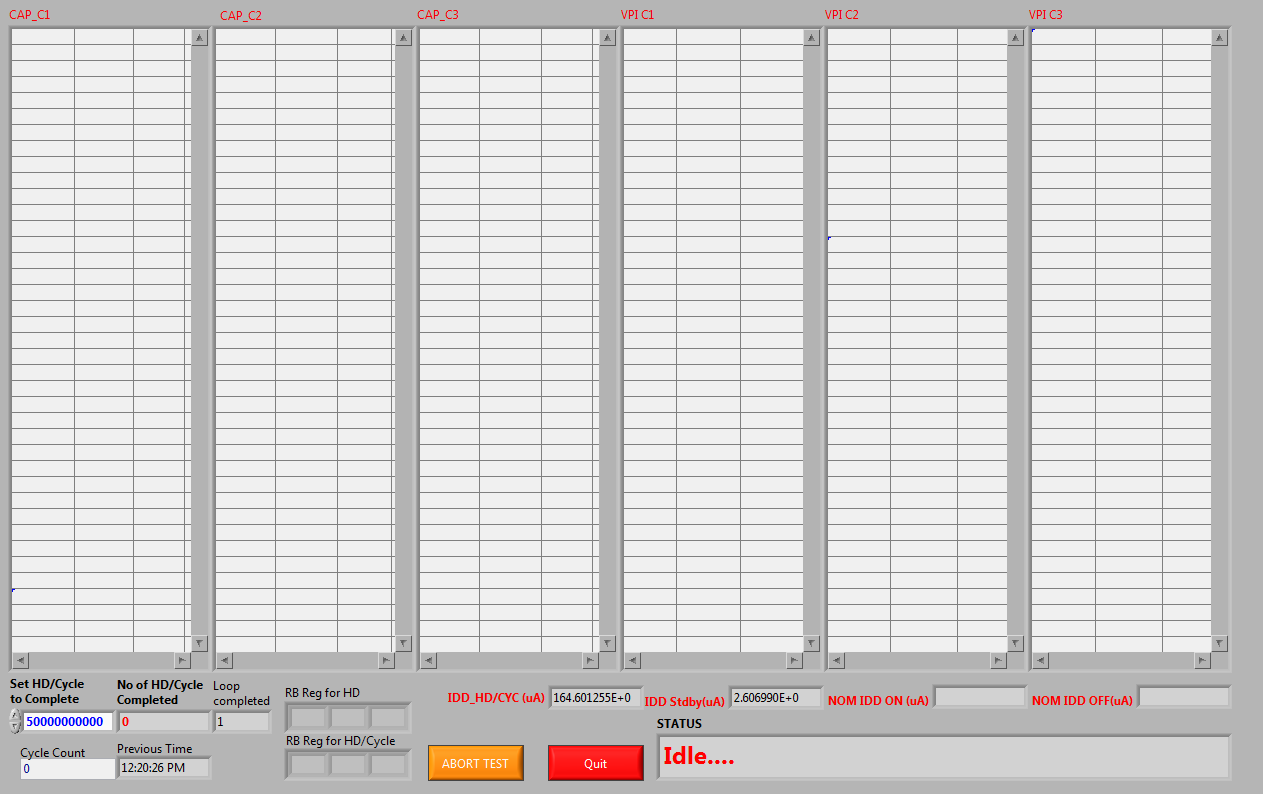
* The test can be set to start immediately by clicking on the START TEST button; alternatively the start date and time can be programmed as shown in Figure 7.



**Figure 7**

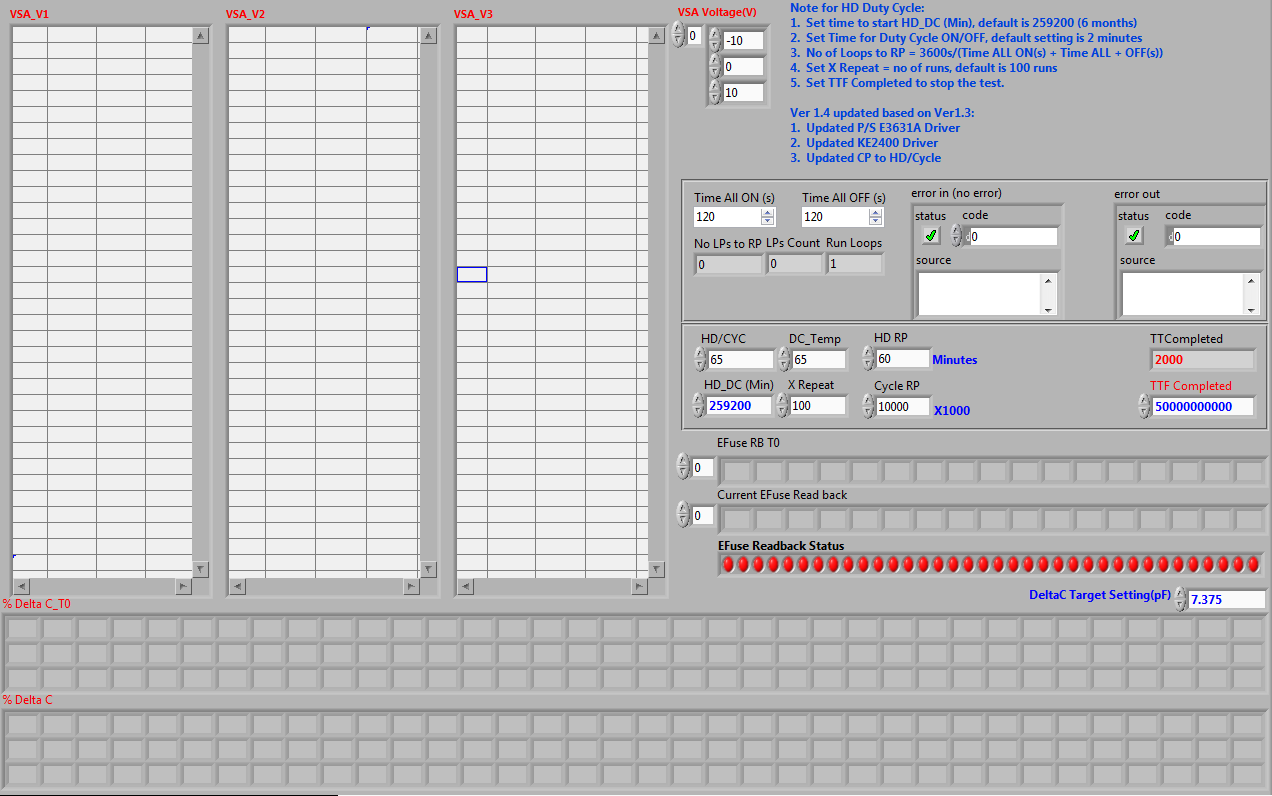
**Note:** **The time shall be set at least 30 minutes to wait after loading parts to the board in the oven/chamber. This time is required for the stabilization of the board dwell time at the temperature before to run stress.**

* The front panel (Figure 8) displays the capacitance values for every read point.



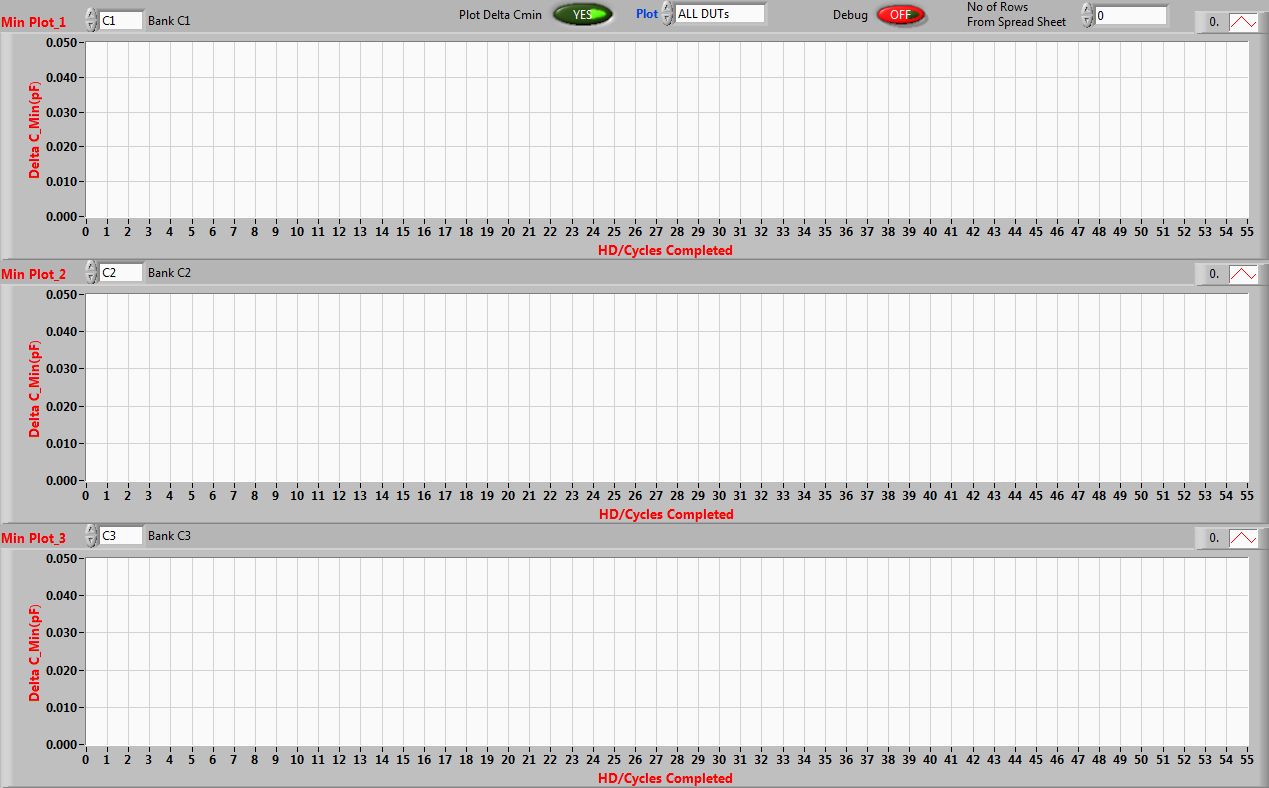
**Figure 8**

* The front panel (Figure 9) displays VSA, HS check, EFUSE, % Delta CAP for every read point



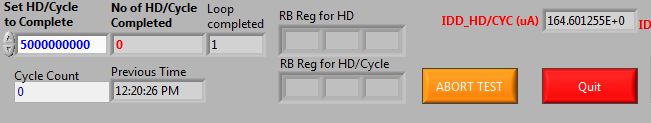
**Figure 9**

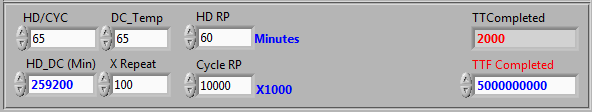
* Figure 10 shows the output results, so that changes in CMIN can be monitored during stress.



**Figure 10**

* Stop stress or abort the test: The test can be aborted immediately by click on the ABORT TEST button (Figure 11) or enter the number that will be set to complete the test (5 billion cycles was set by default).





**Figure 11**

# REVISION HISTORY

|  |  |  |  |
| --- | --- | --- | --- |
| Rev | Description | Editor | Date |
| A | Initial Release | M. Johnson | 12-Aug 2015 |